ABSTRACT OF THE DISCLOSURE

A multiprocessor system is obtained which is capable of efficiently debugging a plurality of processors, while allowing cost reduction. A chip (1) has CPUs (7_0, 7_1), debug executing units (8_0, 8_1), TAP controllers (9_0, 9_1), a selecting circuit (10), and a single set of terminals including terminals (2) to (6). When only the CPU (7_0) is to be debugged, a TAP controller (100) sets a register (101) so that a signal (S11) is "H" and a signal (S12) is "L." When only the CPU (7_1) is to be debugged, the TAP controller (100) sets the register (101) so that the signal (S11) is "L" and the signal (S12) is "H." When both CPUs (7_0) and (7_1) are to be debugged, the TAP controller (100) sets the register (101) so that the signals (S11) and (S12) are both "H."